Exploring Soft ECC Decoding

Growing interest for Software Defined Radio (SDR)

Source Decoder Channel Receiver

Figure 1: Simplified communication chain

- Leverage powerful, energy efficient procs (x86, ARM)
- Reduce dev. cost and time to market
- Validate and optimize new algorithms
- Enable Cloud computing-based architecture for Radio Access Networks (C-RAN)

Recent Successive Cancellation soft decoder for Polar codes [1] strongly benefit from modern CPUs capabilities and SIMD units, open the way to a wide optimization range.

Introducing AFF3CT, a software environment for exploring ECC decoders.

Decoding of Polar Codes

The Successive Cancellation (SC) decoding algorithm: a depth-first binary tree traversal algorithm based on 3 key functions:

\[
\begin{align*}
    f(\lambda_n, \lambda_0) &= \text{sign}(\lambda_n, \lambda_0), \min(|\lambda_n|, |\lambda_0|) \\
    g(\lambda_n, \lambda_{n-1}) &= (1 - 2\lambda_n) + \lambda_{n-1} \\
    h(\lambda_n, s_n) &= (s_n \oplus s_{n-1}) 
\end{align*}
\]

Figure 2: Full SC decoding tree (N = 16)

Conclusion

State of the art SC optimizations and performances
- Inter/intra-frame SIMD implementations
- Generated and dynamic decoders

Energy consumption analysis
- Software SC decoder = only 14 nJ per bit, 65 Mbps (ARM Cortex-A57 @ 1.1GHz, N = 4096, R = 1/2)
- Performance and energy consumption comparison on big.LITTLE ARM32/64 and Intel x86 processors

References


A Fast Forward Error Correction Tool (AFF3CT): Generic ECC Simulation Framework

AFF3CT: a software dedicated to simulations of digital communications with channel coding

http://aff3ct.github.io

- Support many codes: Polar, Turbo, Convolutional, Repeat and Accumulate and LDPC (coming soon)
- Very fast simulations, take advantage of today CPUs architecture (hundreds of Mb/s on Intel Core i5/7)
- Written in C++11 (SystemC/TLM support)
- Monte-Carlo multi-threaded simulations
- From 10 to 1000 faster than MATLAB code
- Portable: run on Linux, Mac OS X and Windows
- Open-source code (under MIT license)

Energy Consumption Analysis of Software Polar Decoders on Low Power Processors

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Figure 3: Simulated BER and FER for the Fast-SCC decoder

Experiments and Measurements

<table>
<thead>
<tr>
<th>Cluster</th>
<th>Impl.</th>
<th>T (µs)</th>
<th>f (MHz)</th>
<th>E (nJ)</th>
<th>P (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7-450MHz</td>
<td>seq.</td>
<td>3.1</td>
<td>655</td>
<td>37.8</td>
<td>0.117</td>
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<tr>
<td>intra</td>
<td>13.0</td>
<td>158</td>
<td>9.5</td>
<td>0.123</td>
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<tr>
<td>inter</td>
<td>21.8</td>
<td>1506</td>
<td>6.0</td>
<td>0.131</td>
<td></td>
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<tr>
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<td>996</td>
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<td>0.082</td>
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<tr>
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<td>7.9</td>
<td>0.070</td>
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<tr>
<td>inter</td>
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<td>1902</td>
<td>5.1</td>
<td>0.088</td>
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<tr>
<td>A15-1.1GHz</td>
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<tr>
<td>intra</td>
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<td>58</td>
<td>28.2</td>
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<tr>
<td>inter</td>
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<td>522</td>
<td>17.4</td>
<td>1.039</td>
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<tr>
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<tr>
<td>inter</td>
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<td>15.8</td>
<td>9.997</td>
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</tr>
</tbody>
</table>

Figure 5: Variation of the energy-per-bit (E_b) depending on the cluster frequency (dynamic code, intra-, inter-frame). A7 performance is on the left and A15 on the right. N = 4096 and R = 1/2. Dark colors and light colors stand for CPU cluster and RAM energy consumption, resp.

Table 1: Characteristics for each cluster (T is the information throughput), for dyn. decoder. N = 4096, rate R = 1/2. The RAM consumption is not included in E_b and in P.

Figure 6: Ranking of the different approaches along 5 metrics. In red, inter-frame vectorization performance and in blue, intra-frame performance. Solid color is for the dynamic versions, dotted is for the generated versions. Each version is sorted along each of the 5 axes and the best version for one axe is placed further from the center.

Contact

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